



## Ultra-Low Power Op Amp in a Tiny 6-Bump WLP

MAX44264

### General Description

The MAX44264 is an ultra-small (6-bump WLP) op amp that draws only 750nA of supply current. It operates from a single +1.8V to +5.5V supply and features ground-sensing inputs and rail-to-rail output. The ultra-low supply current, low-operating voltage, and rail-to-rail output capabilities make these operational amplifiers ideal for use in single lithium ion (Li+), or two-cell NiCd or alkaline battery systems. The rail-to-rail output stage of the MAX44264 is capable of driving the output voltage to within 4mV of the rail with a 100kΩ load, and can sink and source 11mA with a +5V supply. The IC is unity-gain stable and available in a space-saving 0.9mm x 1.3mm, 6-bump WLP package.

### Applications

Cell Phones  
Tablet/Notebook Computers  
Mobile Accessories  
Battery-Powered Devices

### Features

- ◆ Ultra-Low 750nA Supply Current per Amplifier
- ◆ Ultra-Low +1.8V Supply Voltage Operation
- ◆ Ground-Sensing Input Common-Mode Range
- ◆ Outputs Swing Rail-to-Rail
- ◆ Outputs Source and Sink 11mA of Load Current
- ◆ No Phase Reversal for Overdriven Inputs
- ◆ High 120dB Open-Loop Voltage Gain
- ◆ Low 500μV Input Offset Voltage
- ◆ 9kHz Gain-Bandwidth Product
- ◆ 250pF (min) Capacitive Load Capability
- ◆ Available in a Tiny, 0.9mm x 1.3mm, 6-Bump WLP Package

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX44264EWT+	-40°C to +85°C	6 WLP	+CB

+Denotes a lead(Pb)-free/RoHS-compliant package.

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## ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub> to V<sub>SS</sub> .....-0.3V to +6V  
 IN<sub>+</sub> or IN<sub>-</sub>.....(V<sub>SS</sub> - 0.3V) to (V<sub>DD</sub> + 0.3V)  
 OUT<sub>-</sub> Shorted to V<sub>SS</sub> or V<sub>DD</sub>.....Continuous  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
 6-Bump WLP (derate 10.5mW/°C above +70°C) .....840mW

Operating Temperature Range ..... -40°C to +85°C  
 Junction Temperature ..... +150°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C  
 Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +5V, V<sub>SS</sub> = 0V, V<sub>CM</sub> = 0V, V<sub>OUT</sub> = V<sub>DD</sub>/2, R<sub>L</sub> = ∞ to V<sub>DD</sub>/2, T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Supply Voltage Range	V <sub>DD</sub>	Guaranteed by PSRR tests	1.8		5.5	V	
Supply Current (per Amplifier)	I <sub>DD</sub>	V <sub>DD</sub> = +1.8V		0.6		μA	
		V <sub>DD</sub> = +5.0V		0.75	1.2		
Input Offset Voltage	V <sub>OS</sub>			±0.5	±7.0	mV	
Input Bias Current	I <sub>B</sub>			±200	±1500	pA	
Input Offset Current	I <sub>OS</sub>			±12.5		pA	
Input Common-Mode Voltage Range	V <sub>CM</sub>	Guaranteed by the CMRR test	V <sub>SS</sub>		V <sub>DD</sub> - 1.1	V	
Common-Mode Rejection Ratio	CMRR	Specified with V <sub>SS</sub> ≤ V <sub>CM</sub> ≤ (V <sub>DD</sub> - 1.1V)	70	95		dB	
Power-Supply Rejection Ratio	PSRR	+1.8V ≤ V <sub>DD</sub> ≤ +5.5V	70	90		dB	
Large-Signal Voltage Gain	A <sub>VOL</sub>	R <sub>L</sub> = 1MΩ, V <sub>OUT</sub> = 50mV to V <sub>DD</sub> - 50mV	90	120		dB	
		R <sub>L</sub> = 100kΩ, V <sub>OUT</sub> = 200mV to V <sub>DD</sub> - 200mV	90	112			
		R <sub>L</sub> = 10kΩ, V <sub>OUT</sub> = 200mV to V <sub>DD</sub> - 200mV		100			
Output Voltage Swing	V <sub>OH</sub>	Swing high specified as V <sub>DD</sub> - V <sub>OH</sub>	R <sub>L</sub> = 1MΩ		1	4	mV
			R <sub>L</sub> = 100kΩ		4	10	
			R <sub>L</sub> = 10kΩ		40		
	V <sub>OL</sub>	Swing low specified as V <sub>OL</sub> - V <sub>SS</sub>	R <sub>L</sub> = 1MΩ		0.5	5	
			R <sub>L</sub> = 100kΩ		1	5	
			R <sub>L</sub> = 10kΩ		10		
Gain-Bandwidth Product	GBW			9		kHz	
Phase Margin	φ <sub>M</sub>			90		degrees	

# Ultra-Low Power Op Amp in a Tiny 6-Bump WLP

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L = \infty$  to  $V_{DD}/2$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	SR	$V_{OUT} = 4V$ step		2		V/ms
Input Voltage Noise	$e_n$	$f = 1kHz$		150		$nV/\sqrt{Hz}$
		$f = 10kHz$		120		
Output Short-Circuit Current		Shorted to $V_{SS}$ (sourcing)		11		mA
		Shorted to $V_{DD}$ (sinking)		36		
Power-On Time	$t_{ON}$			2		$\mu s$
Power-Off Time	$t_{OFF}$			2		$\mu s$
Capacitive Load	$C_{LOAD}$	No sustained oscillations	250			pF

## ELECTRICAL CHARACTERISTICS

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L = \infty$  to  $V_{DD}/2$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.) (Note 1)

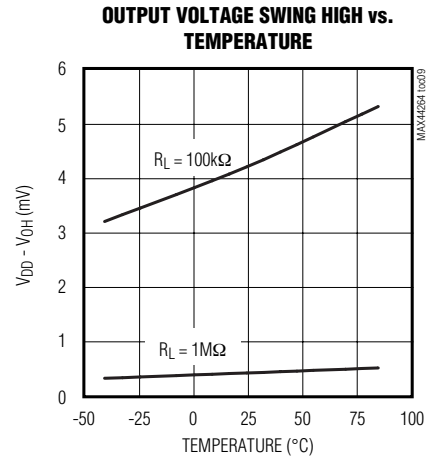
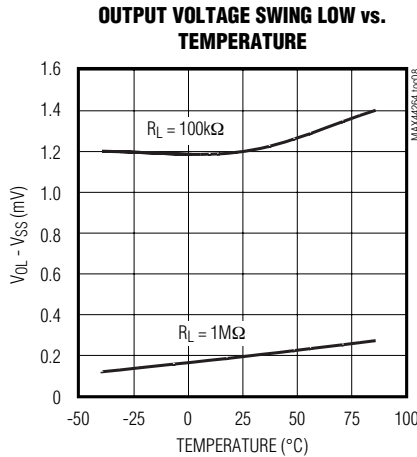
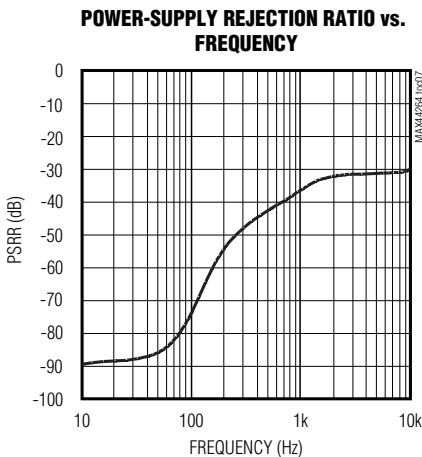
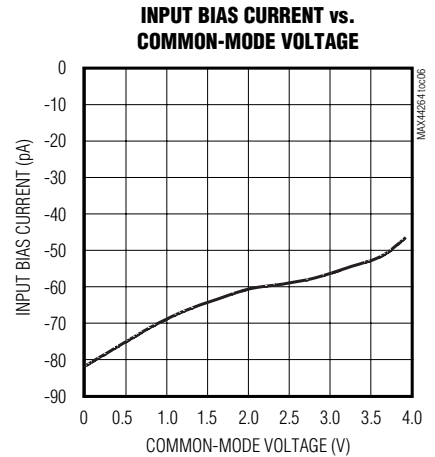
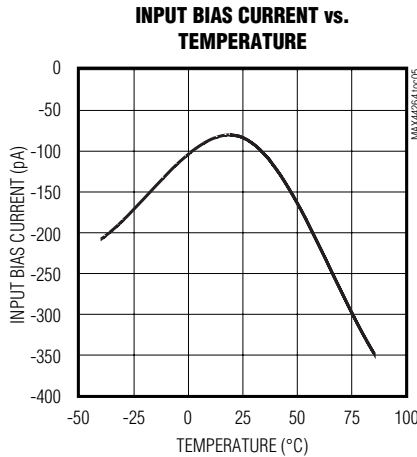
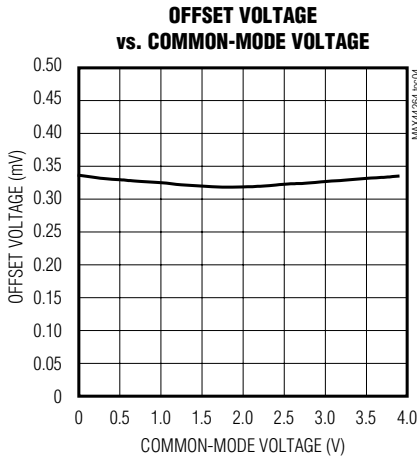
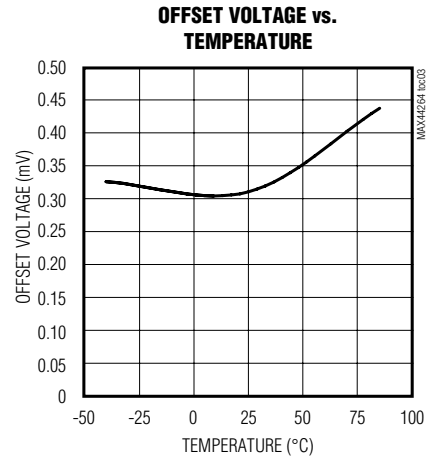
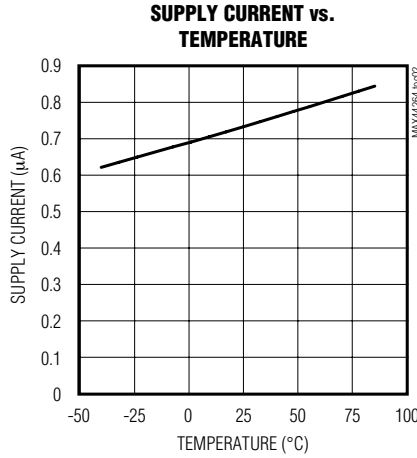
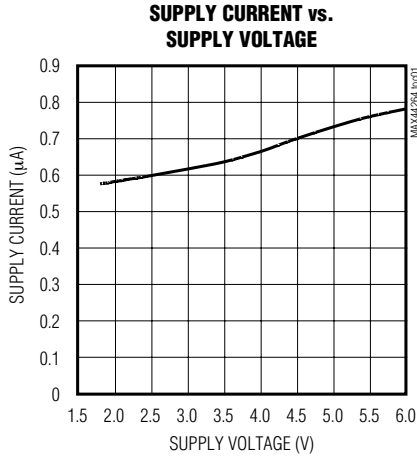
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	$V_{DD}$	Guaranteed by PSRR tests	1.8		5.5	V
Supply Current (per Amplifier)	$I_{DD}$	$V_{DD} = +5.0V$			1.5	$\mu A$
Input Offset Voltage	$V_{OS}$				$\pm 15$	mV
Input Offset Voltage Temperature Coefficient	$TCV_{OS}$			8		$\mu V/^\circ C$
Input Bias Current	$I_B$				4.25	nA
Input Common-Mode Voltage Range	$V_{CM}$	Guaranteed by the CMRR test	$V_{SS}$		$V_{DD} - 1.1$	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} \leq V_{CM} \leq (V_{DD} - 1.1V)$	56			dB
Power-Supply Rejection Ratio	PSRR	$+1.8V \leq V_{DD} \leq +5.5V$ , $0^\circ C \leq T_A \leq +85^\circ C$	65			dB
		$+2V \leq V_{DD} \leq +5.5V$ , $-40^\circ C \leq T_A \leq +85^\circ C$	65			
Large-Signal Voltage Gain	$A_{VOL}$	$V_{OUT} = 50mV$ to $V_{DD} - 50mV$ , $R_L = 1M\Omega$	75			dB
		$V_{OUT} = 200mV$ to $V_{DD} - 200mV$ , $R_L = 100k\Omega$	75			
Output Voltage Swing	$V_{OH}$	Swing high specified as $V_{DD} - V_{OH}$	$R_L = 1M\Omega$		5	mV
			$R_L = 100k\Omega$		15	
	$V_{OL}$	Swing low specified as $V_{OL} - V_{SS}$	$R_L = 1M\Omega$		5	
			$R_L = 100k\Omega$		5	

**Note 1:** All devices are production tested at  $T_A = +25^\circ C$ . All temperature limits are guaranteed by design.

# Ultra-Low Power Op Amp in a Tiny 6-Bump WLP

## Typical Operating Characteristics

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $R_L = 100k\Omega$  to  $V_{DD}/2$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



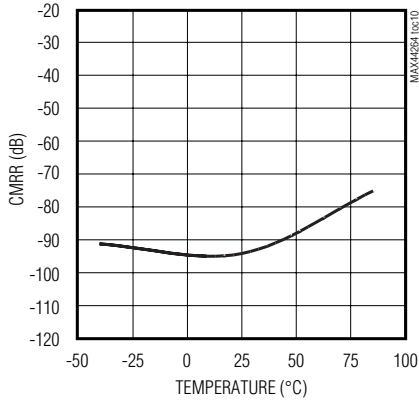
# Single/Dual/Quad, +1.8V/750nA, SC70, Rail-to-Rail Op Amps

MAX44264

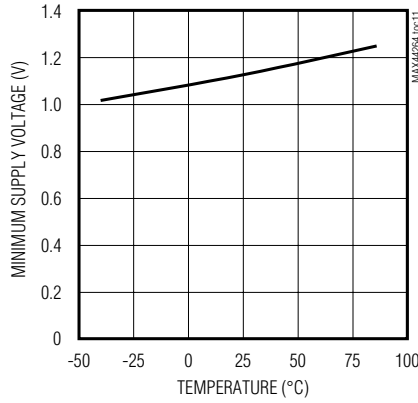
## Typical Operating Characteristics (continued)

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $R_L = 100k\Omega$  to  $V_{DD}/2$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

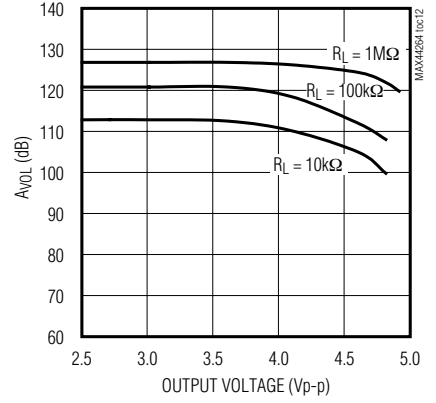
**COMMON-MODE REJECTION RATIO vs. TEMPERATURE**



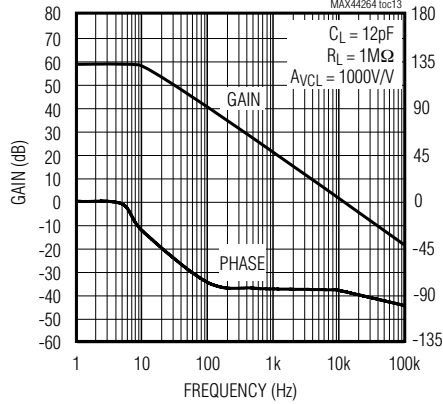
**MINIMUM SUPPLY VOLTAGE vs. TEMPERATURE**



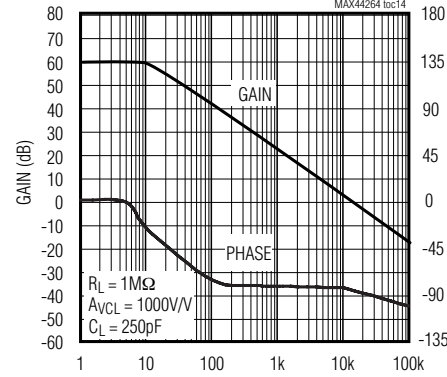
**AvOL vs. OUTPUT VOLTAGE SWING**



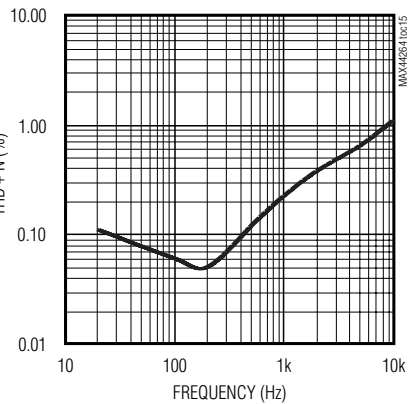
**GAIN AND PHASE vs. FREQUENCY**



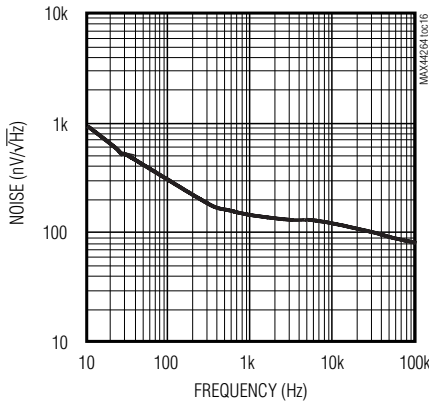
**GAIN AND PHASE vs. FREQUENCY**



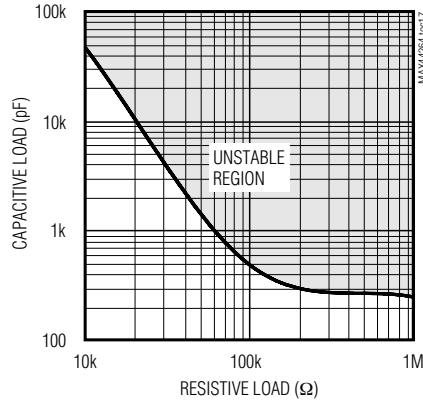
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**



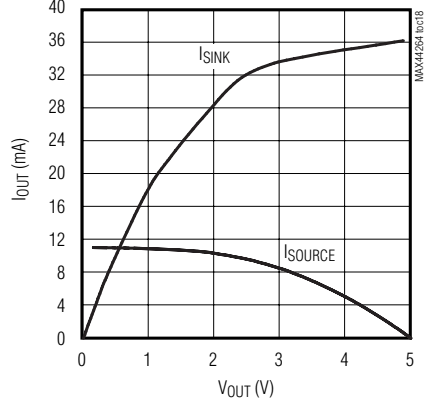
**VOLTAGE NOISE DENSITY vs. FREQUENCY**



**STABILITY vs. CAPACITIVE AND RESISTIVE LOADS**



**IOUT vs. VOUT**

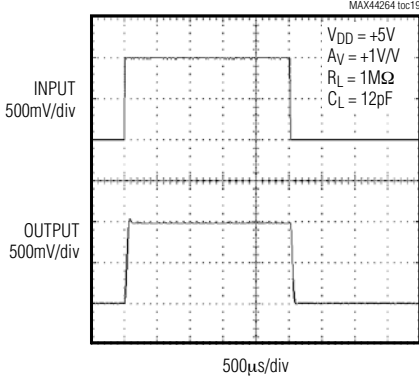


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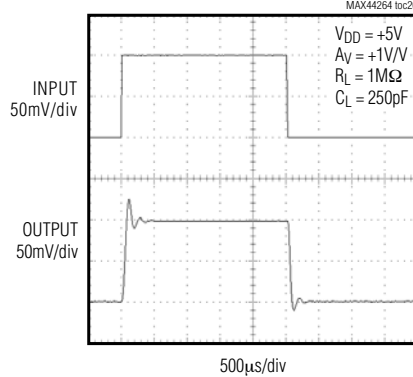
## Typical Operating Characteristics (continued)

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $R_L = 100k\Omega$  to  $V_{DD}/2$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

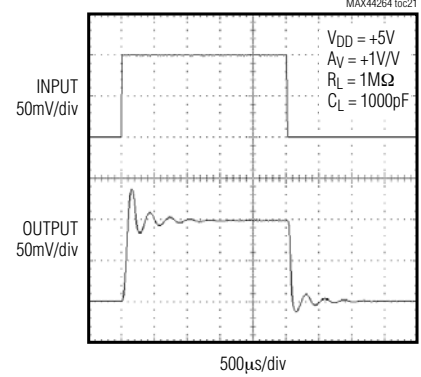
**SMALL-SIGNAL STEP RESPONSE**



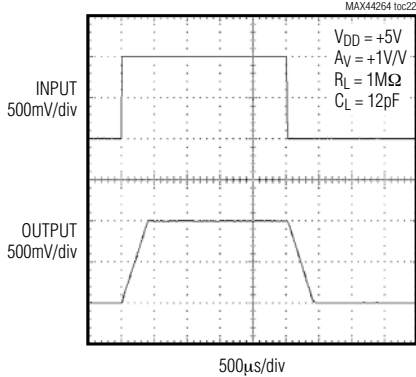
**SMALL-SIGNAL STEP RESPONSE**



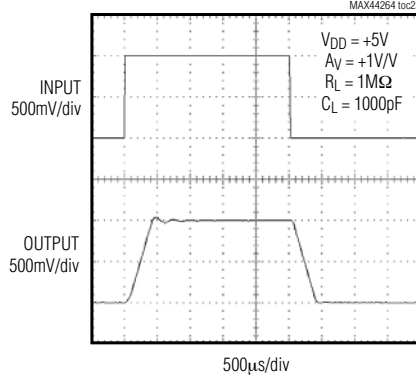
**SMALL-SIGNAL STEP RESPONSE**



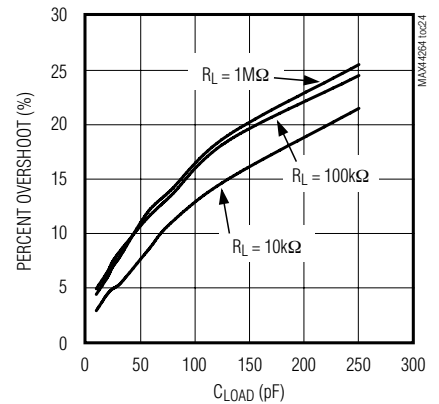
**LARGE-SIGNAL STEP RESPONSE**



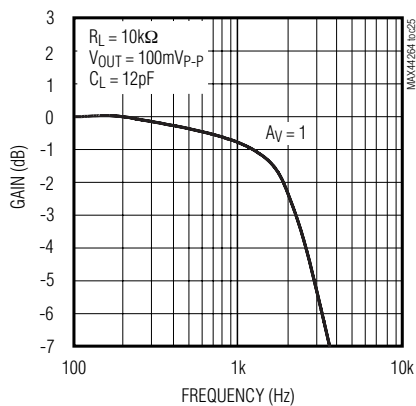
**LARGE-SIGNAL STEP RESPONSE**



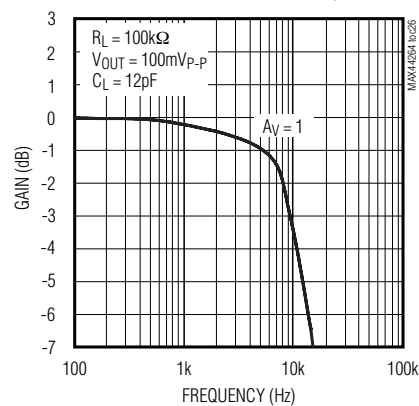
**PERCENT OVERSHOOT vs. CAPACITIVE LOAD**



**SMALL-SIGNAL GAIN vs. FREQUENCY**



**SMALL-SIGNAL GAIN vs. FREQUENCY**

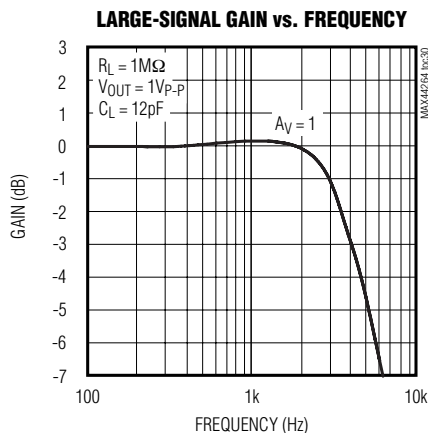
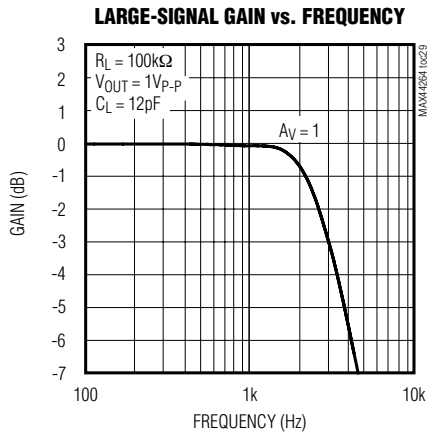
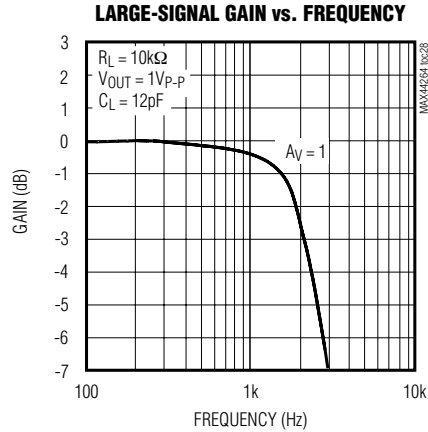
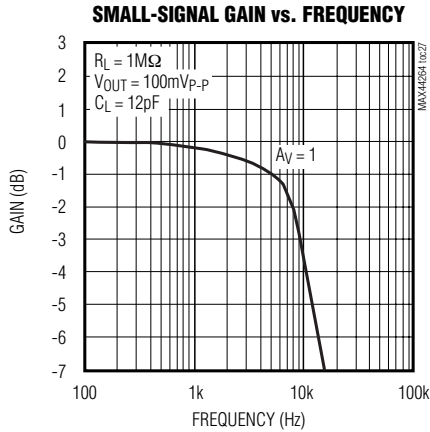


# Ultra-Low Power Op Amp in a Tiny 6-Bump WLP

## Typical Operating Characteristics (continued)

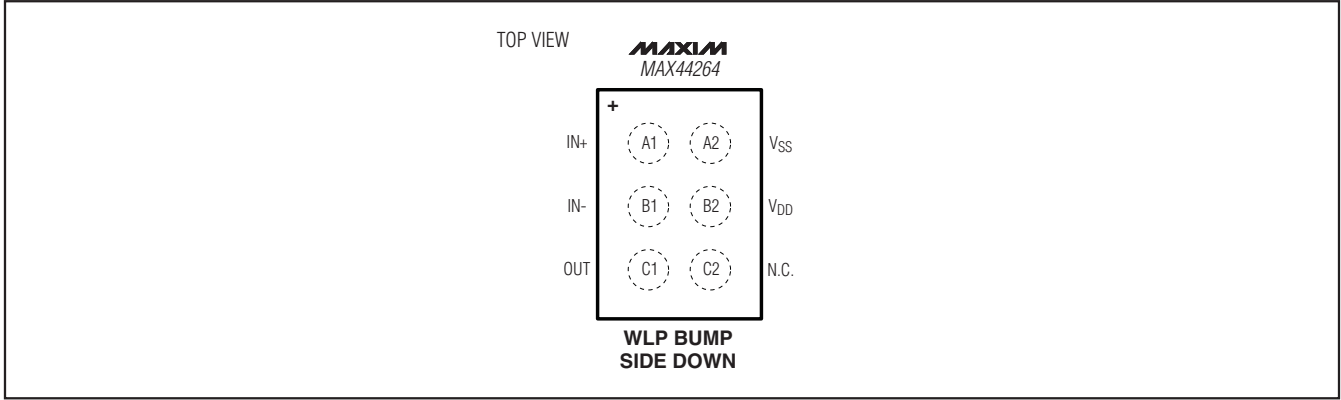
( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $R_L = 100k\Omega$  to  $V_{DD}/2$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX44264



# Ultra-Low Power Op Amp in a Tiny 6-Bump WLP

## Pin Configuration



## Pin Description

PIN	NAME	FUNCTION
A1	IN+	Noninverting Amplifier Input
A2	V <sub>SS</sub>	Negative Power-Supply Voltage
B1	IN-	Inverting Amplifier Input
B2	V <sub>DD</sub>	Positive Power-Supply Voltage
C1	OUT	Amplifier Output
C2	N.C.	No Connection. Not internally connected.

## Applications Information

### Ground Sensing

The common-mode input range of the MAX44264 extends down to ground, and offers excellent common-mode rejection. These devices are guaranteed not to undergo phase reversal when the input is overdriven.

### Power Supplies and Layout

The IC operates from a single +1.8V to +5.5V power supply. Bypass power supplies with a 0.1μF ceramic capacitor placed close to the V<sub>DD</sub> pin.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the op amp's inputs and outputs. To decrease stray capacitance, minimize PCB lengths and resistor leads, and place external components close to the op amps' pins.

### Bandwidth

The IC is internally compensated for unity-gain stability and has a typical gain-bandwidth of 9kHz.

### Stability

The IC maintains stability in their minimum gain configuration while driving capacitive loads. Although this product family is primarily designed for low-frequency

applications, good layout is extremely important because low-power requirements demand high-impedance circuits. The layout should also minimize stray capacitance at the amplifier inputs. However some stray capacitance may be unavoidable, and it may be necessary to add a 2pF to 10pF capacitor across the feedback resistor as shown in Figure 1. Select the smallest capacitor value that ensures stability.

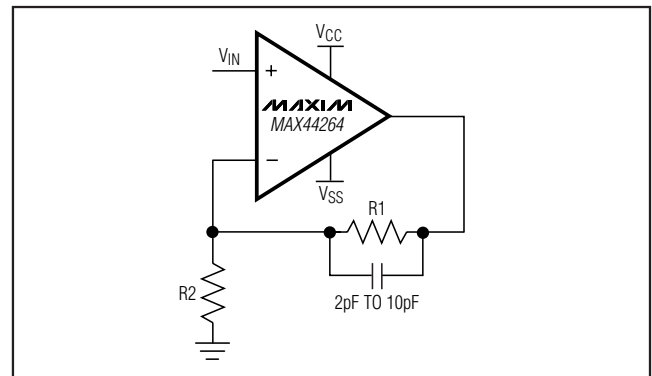


Figure 1. Compensation for Feedback Node Capacitance

## Chip Information

PROCESS: BiCMOS



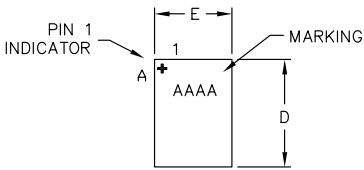
# Ultra-Low Power Op Amp in a Tiny 6-Bump WLP

MAX44264

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 WLP	W61B1+1	<a href="#">21-0217</a>	—

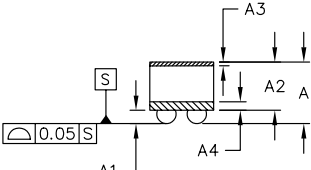


PIN 1 INDICATOR

MARKING

AAAA

TOP VIEW



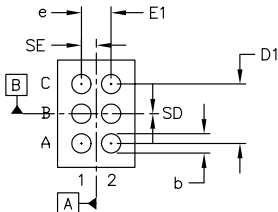
SIDE VIEW

COMMON DIMENSIONS	
A	0.64±0.05
A1	0.19±0.03
A2	0.45 REF
A3	0.025 BASIC
A4	0.07 BASIC
b	∅0.27±0.03
D1	0.80 BASIC
E1	0.40 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.20 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W61B1+1	0.76	0.97	1.17	1.37	NONE
W61D1+1	0.95	1.02	1.36	1.42	NONE


NOTES:

- Terminal pitch is defined by terminal center to center value.
- Outer dimension is defined by center lines between scribe lines.
- All dimensions in millimeters.
- Marking shown is for package orientation reference only.
- Tolerance is ± 0.02mm unless specified otherwise.
- All dimensions apply to PbFree (+) package codes only.



BOTTOM VIEW

—DRAWING NOT TO SCALE—



TITLE: PACKAGE OUTLINE 6 BUMPS, WLP PKG. 0.4mm PITCH		
APPROVAL	DOCUMENT CONTROL NO. 21-0217	REV. B 1/1

# **Ultra-Low Power Op Amp in a Tiny 6-Bump WLP**

## **Revision History**

<b>REVISION NUMBER</b>	<b>REVISION DATE</b>	<b>DESCRIPTION</b>	<b>PAGES CHANGED</b>
0	12/10	Initial release	—

*Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.*

**10** \_\_\_\_\_ **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**